GaAs and GaN MESFETs and HFETs Processing Technology and Reliability Relationships, A Review

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ABSTRACT

Although accelerated life testing of low noise and power GaAs MESFETs under d.c. bias and RF operation has been conducted, some failure mechanisms remain to be of concern. We will address these concerns and will develop failure models to include AlGaAs/GaAs HFETs. The new set of reliability physics models then will form the starting point for development of physics based failure models for GaN HFETs devices. Processes in effect in GaN, but not in GaAs, owing to higher fields and much larger field, temperature, and strain coupling will be included. In this vein, we discuss the state of the art of testing and failure mode analyses of GaAs devices and comment on the relevance to the proposed work. The same philosophy will then be extended to GaN based HFETs.

A dominant failure mode of power GaAs MESFETs is catastrophic burn-out which is difficult to interpret. The 'long-term' catastrophic failure is the final result of parametric degradation while the 'instantaneous' burn-out is caused by sudden events, typically electrical overstress. Other failure mechanisms inducing parametric degradation are surface degradation, backgating, gate electromigration, and degradation of Schottky and ohmic contacts. The status for GaN is much less clear since gate leakage and the combined effects of high field, heat, and strain are all inter related and combined may cause the 'instantaneous' burn-out. Only after these mechanisms are minimized, can the 'long-term' parametric degradation become evident.

1.1.a. Failure Modes and Mechanisms of GaAs MESFETs

Surface states lower the maximum field in the gate drain region, due to the captured negative charge which decreases the impact ionization, and increases the gate-drain breakdown voltage, V_B. Deep levels associated with surface states result in 'gate-lag' and transconductance dispersion which are strongly correlated since the characteristic capture and release times of surface states are longer than that of the applied signal. The magnitude of gate-lag and $g_m(f)$ dispersion is proportional to the surface state density.[1] Gate-drain burn-out is caused by avalanche breakdown which depends on surface characteristics and device layout and technology. A recessed gate design would improve it. Source-drain burn-out is of thermal origin at the drain contact, a remedy for which is the n^+ drain edge geometry resulting in uniform current flow and current spreading. The burn out might be dominated by the substrate/buffer region reaching extreme temperatures leading to the sudden increase in drain current.[1] These phenomena are expected to occur in GaN HFETs as well, and the detailed analyses is necessary in order to develop the appropriate degradation model.

1.1. b Failure Modes and Mechanisms of AlGaAs/GaAs HFETs

The AlGaAs/GaAs HFET degradation mechanisms, beyond those for GaAs MESFETs, include deep levels in the barrier and changes in the 2DEG concentration. The I-V collapse in the dark, and persistent photo-conductivity are more related to the material quality than to the long-term device stability. The decrease in 2DEG density might be due to carrier de--confinement, enhanced by field-aided impurity diffusion at the heterointerface (would also occur in GaN HFETs). The defects, present or created by high field (temperature, strain) followed by hot electron capture, would reduce the available carriers. These anomalies also cause high levels of LF noise. Similar effects must undoubtedly take place in the GaN system. Extensive analyses coupled with test heterostructures will be undertaken to uncover the nature of these anomalies for the failure model development.

Electromigration plays an important role in GaAs HFETs since GaAs,[1] being a binary compound, may have a wide variety of surface conditions (various native oxides and their clusters, surface states etc.). Further, electromigration is influenced by conductor-line material parameters and inhomogeneities, as well as structural features of the conductor layout, etc. Avoidance of sharp corners or transitions from a wide conductor to a narrow one helps mitigate the problem. Therefore, the electromigration effect must be studied with the same microscopic geometries as those used for both GaAs and GaN devices and knowledge gained will be applied to the physics based reliability models.

2. GaN FET physics of failure/degradation

The degradation mechanisms germane to GaN, in addition to those present in GaAs, are primarily related to surface traps, metal semiconductor and inter-metal diffusion, compound formation, interface and bulk defect states. However, local high fields (>> GaAs) coupled with strain and temperature as well as the increased hot phonon generation will alter the key GaN HFET degradation mechanisms. Clearly, the GaAs model can be a starting point to be followed with its expansion to incorporate the GaN specific mechanisms. A variety of "trap" related device effects have been observed which include transconductance frequency dispersion, current collapse, light sensitivity, gate- and drain-lag transients, and restricted microwave power output.[1] The preliminary activity directed toward characterizing these effects[2] parallels similar developments in the GaAs-based technology.

Electron capture-emission by surface and bulk traps affects the 2DEG density resulting in current collapse, and transconductance dispersion. Because the associated characteristic time is ~ $1ns<\tau<1$ s, the trapping limits device performance even at relatively low frequencies. In addition, the thermally activated traps contribute significantly to LF noise. Understanding the origin of the traps in GaN-based transistors, their physical and energy location, and the physical mechanisms involved in the trapping is critical for not just the optimization of device performance, but for reliability modeling and reliability optimization for the GaN HFETs. We report (Figure 1) on the study of the nature of bulk (GaN and AlGaN), surface states, and interface states along with their effects on gate leakage followed by the effect of passivation, including the in situ deposited Si_3N_4. Degradation caused by surface states and preexisting bulk and interface states are reversible. However, when new defects begin to be created and their density cascades due to the combined effects of high field, heat and strain, the resulting device degradation becomes catastrophic.

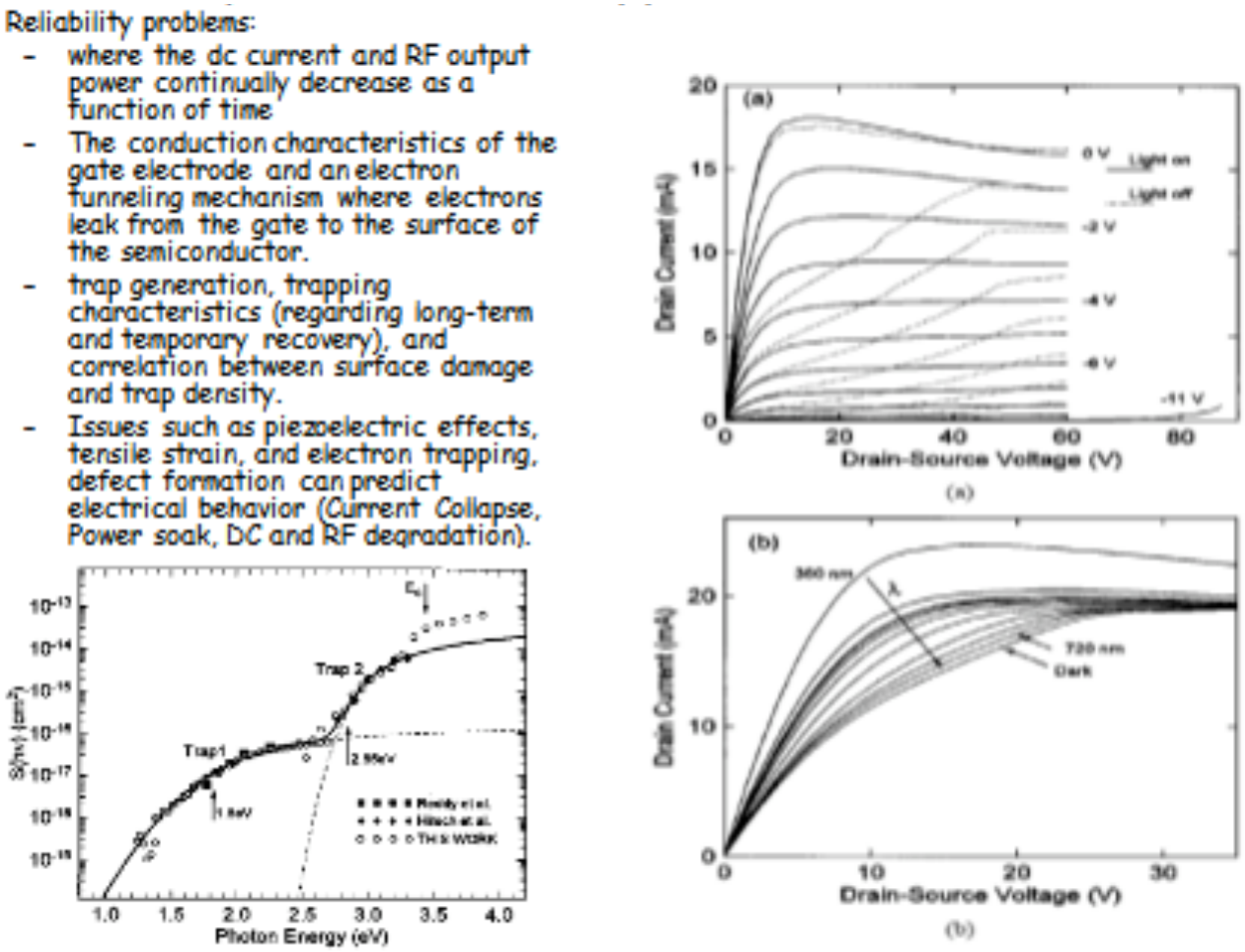

Figure 1. Figures showing the location of two traps as well as the drain current collapse with wavelength.

2.1 Bulk buffer traps

Bulk traps in early GaN MESFETs and HFETs have been investigated.[4] The fitted photoionization thresholds located the two dominant defects at ~ 1.80 and 2.85 eV below the conduction band edge, and after the 0.55 eV and 0.2 eV Franck-Condon correction, respectively. The DX centers plausibly associated with O have been observed in AlGaN may also be present. The enhancement of the optically induced drain-current recovery for photon energies at or above the band gap, E_g, of GaN has been measured and in contrast, no such increase for photon energies above E_g of AlGaN has been observed, hence, placing the traps to be within GaN buffer layer. However, it is obvious that further investigations are necessary. For instance, Trap 2 appears to be correlated with MOCVD growth pressure since trap 2 density increases at lower pressures. *Obviously, this area requires further insightful investigations in order to determine the nature of the traps present.*

2.2 Bulk Barrier traps

Bulk barrier defects results in the trapping of carriers injected from the gate and/or hot carriers injected from the channel and leads to current reduction by reducing 2DEG density. The lateral and vertical fields also enhance the charge emission from the barrier traps. The field effects, therefore, are particularly

important and must be taken into account. Localized trapping centers within the bandgap in the vicinity of the gate where the gate potential defines the energy position of the trap level with respect to the Fermi level have been investigated.[1] The trap levels depend on the Al mole fraction. Activation energies and concentration of the traps must be determined with respect to Al mole fraction and incorporated into the failure model.

2.3. Surface traps

A strong correlation of gate lag with the surface treatment suggests that at least some trapping centers, besides the bulk GaN and AlGaN traps, are located at or near the surface. Surface trapping can be identified by measuring gate lag for a devices with different surfaces achieved by chemical treatment or dielectric passivation. The temporal character of charge emission from these traps is typically a stretched exponent with a characteristic time in the range of seconds. Practically no quantitative investigation exists because of difficulties of the analysis of the stretched exponent dynamics. Kelvin probe microscopy showed that electrons migrate 0.5–1 μm along the surface away from the gate.[Error! Bookmark not defined.] An area of particular concern is the limiting effect of electronic traps on RF performance. Electrostatic force and Kelvin probe microscopes can measure both local surface charge and potential with high spatial resolution[1,2] Traps form quasi-static charge distributions, most notably on the wafer surface or in the buffer layers underlying the active channel, act to restrict the drain-current and voltage excursions.[3,4,5]

2.4 Interface defects: Heterojunction quality including the effect of AlN interface layer

The barrier/buffer interface is critical for device reliability. Imperfections in as grown material and those created during high field/temperature stresses can in fact be the source of the increased channel resistance. The wavefunction overlap with the barrier makes transport susceptible to the quality of the barrier and thus the defects. Hot carrier injection into the barrier will result in damage and will reduce the available channel conductance locally, leading to local heating and when combined with high fields to enhanced defect generation. To combat electron injection and the resulting anomalies, an AlN interfacial layer is introduced. Indeed the mobility measurements confirm the expected improvement. However, under RF stress nearly ¾ of devices having AlN interface layer as opposed nearly 1/3 of those without it showed degradation.[3] *The bulk and interface defects that are generated due to the coupled forces of electric field, temperature and strain and which play a dominant role in device degradation have not been studied in detail and require further investigations.*

2.5 Hot phonon effects

Existing defects and those generated by hot phonons and electrons, and high fields cause G-R noise[4] which can be monitored with LF noise measurements.[5,6,7] This together with hot phonon effects (with temperature reaching 2000 K at 50-60 kV/cm),[8, 9] accessed by HF noise measurements and simulations,[8] will be used to determine the nature of these defects as input for physics based modeling of failure. Strong electron-phonon coupling in GaN[10] leads to hot phonon generation (some 30 X greater *vs.* GaAs) which is assisted by the inefficient LO phonon decay mechanism. The hot phonon/electron damage and phonon decay mechanisms which are also critically important for heat dissipation are not developed in GaN. The combined effects of high electric field, hot phonons, thermal (heat), mechanical (strain), polarization (charge) will be investigated for the reliability model development.

3. Gate leakage and its impact on reliability

The best performance GaN HFETs is inconsistently obtained with significant dispersion from device-to-device, and from wafer-to-wafer. All high voltage GaN HFETs are affected and the problem is more severe as the device is scaled to reduced dimensions and the operating frequency is increased. The evolution of current and RF power reduction is generally a reversible process. However, the reliability is a strong function of gate leakage current, and that a 'sudden reliability' problem[11] exists when the field reaches a critical value, leading to permanent catastrophic damage. This has been attributed electron tunneling from the gate (drain side) to the surface, particularly when subjected to high terminal voltages.[Error! Bookmark not defined.] It is shown that the reliability problem is due to electrons leaking from the gate electrode to the surface of the semiconductor.[12]

3.1. Ohmic and Schottky contacts

GaN devices push metallization stability to their limit resulting in metallization degradation. Both the gate and drain/source metallurgy change including metallurgical phase change which is progressive and irreversible. Therefore, any complete model must take phase transformations and metal degradation into account.

The Ti/Al contacts are initially stable against oxidation and cracking when sealed with Ni/Au[13] but degrade after prolonged operation. This is a wearout mechanism which can be rapidly revealed by accelerated life tests. Ultimately, an n^+ top layer on AlGaN barrier and gate recessing would be required to reduce contact resistivity and ensure current uniformity. Selective dry etching for gate recessing have already been explored.[14,15] These concepts will be incorporated into test structures and devices by the industrial partner. Interdiffusion at metallic interfaces and possible electromigration from contact regions also produce defect generation which degrades the device performance. These processes must be properly modeled and simulated to determine the critical bias and channel current conditions which crucially affect the rate of the device degradation. Using TEM microdiffraction analyses concurrently with the life tests, degradation mechanisms will be determined and used for input into the model development.

3.2 Field-assisted metal diffusion

The extent of electromigration is dependent on factors such as conductor-line properties and any inhomogeneities as well as structural features of the conductor layout. Naturally, electromigration must be studied since the magnitude of defect transfer depends directly on the current density and poses a formidable challenge for GaN FETs. High temperatures, particularly by the gate and drain metallization, will result in mass transport facilitated by the short diffusion distance associated with defects, such as dislocations, grain boundaries, or external surfaces. It is therefore imperative that we study and understand fully the mechanisms for electromigration and interdiffusion and transfer this knowledge to our reliability models.

3.3 Conclusions

Our effort will culminate in the development of physics based failure models for GaAs and GaN based FETs. More important this project will establish an integrated fundamental science approach encompassing degradation processes such as the material/heterostructures, bulk, surface and interface states, temperature, strain, and high field effects such as hot carriers and hot phonons generation as well

the materials science of contacts and Schottky barriers. The point defect parameters and their effect on device reliability will be determined accurately which will include surface, interface, bulk barrier and bulk buffer traps. We will uncover the physics of hot phonons and hot electrons and their interplay with thermal and polarization phenomena as well as interactions with existing defects and the nucleation of new defects. The effect of hot electron and hot phonon on phonon decay and power dissipation as well as the velocity limiting processes will be determined accurately. The nature of gate leakage current and its effect on reliability, which is somewhat temporary with long recovery time, will be determined.

The effort will lead to a comprehensive reliability physics model (drift-diffusion, electro-thermal, hot-phonon, and Boltzmann transport and charge control), which does not yet exist. The effort will lead to the effective parametization of the degradation mechanisms. With appropriate probability density functions the model will predict statistically meaningful lifetimes. We expect to develop a set of radiation hardness methodologies, inclusive of radiation simulation computational tools to predict the effects of single events as well as to the susceptibility to degradation from ionizing radiation, for the GaN HFET technology. The project results will allow for the rapid insertion of this technology in space systems. The above will culminate in a new charge control model to be developed that can be integrated with RF CAD tools and circuit simulators, which will simulate device degradation, especially for such phenomena as the IV collapse and the kink effect

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