Flexible Displays With Nanostructured Integrated Power Sources

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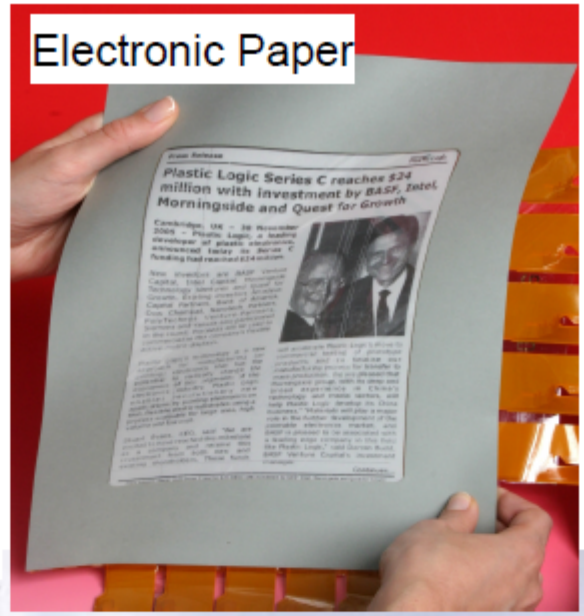
Applications for Flexible Hybrid Electronics

- ✧Energy
  - Photovoltaics
  - Solid-State Lighting
  - Batteries
- ✧Electronics
  - Displays
  - e-Paper
  - Sensors & Actuators
- ✧Biomedical and Healthcare
- ✧Communications
  - -RFID
- ✧Defense

Motivation for Flexible Electronics

RFID Tags Everywhere



Electronic Paper

Wearable Electronics

Large Area Displays

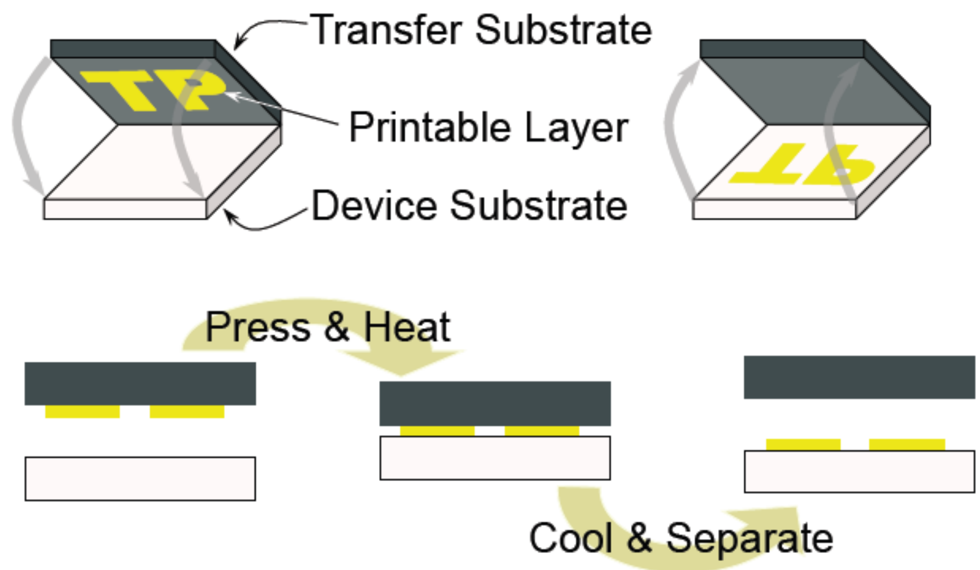
Most Promising Fabrication Methods

Fabrication methods for Flexible Electronics

- Photolithography
- Ink-jet printing
- Gravure
- Flexography
- Screen Printing
- Contact Printing / Soft Lithography
- Nano-Imprinting / Transfer Printing
- Laser-based approaches
- Roll-to-Roll

- ► Transfer Printing
- ► Photolithography with LT Processing

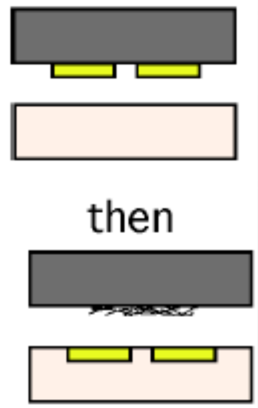
Transfer Printing



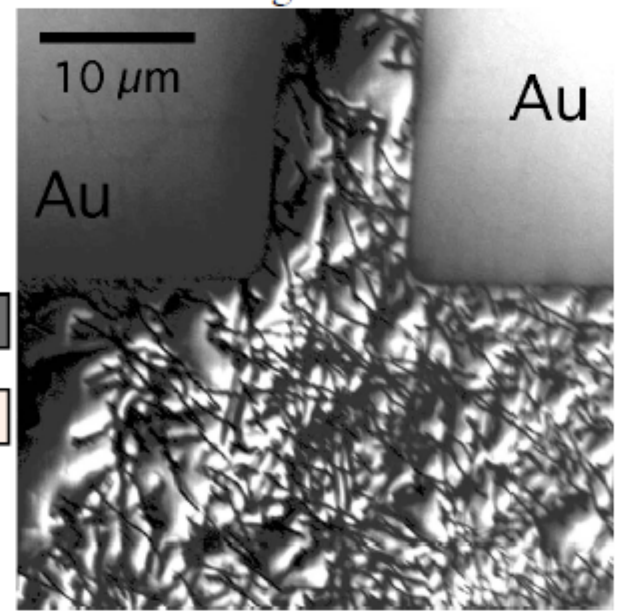
Relies on **Differential Adhesion**:
Printable Layer must be more adhesive to Device Substrate than to Transfer Substrate

Successful Implementation of Transfer Printing

Carbon Nanotubes
Printed
onto
Plastic

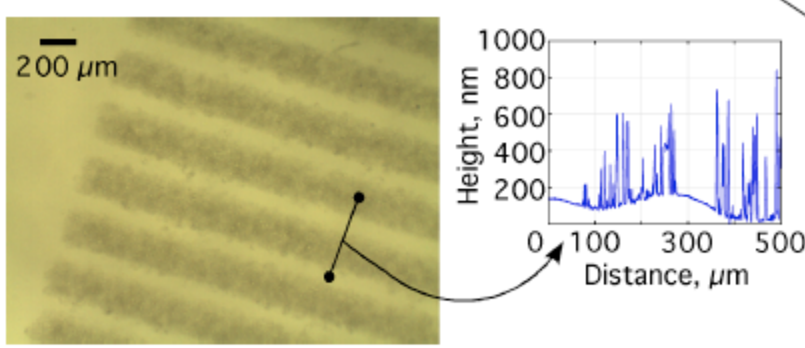


SEM Image



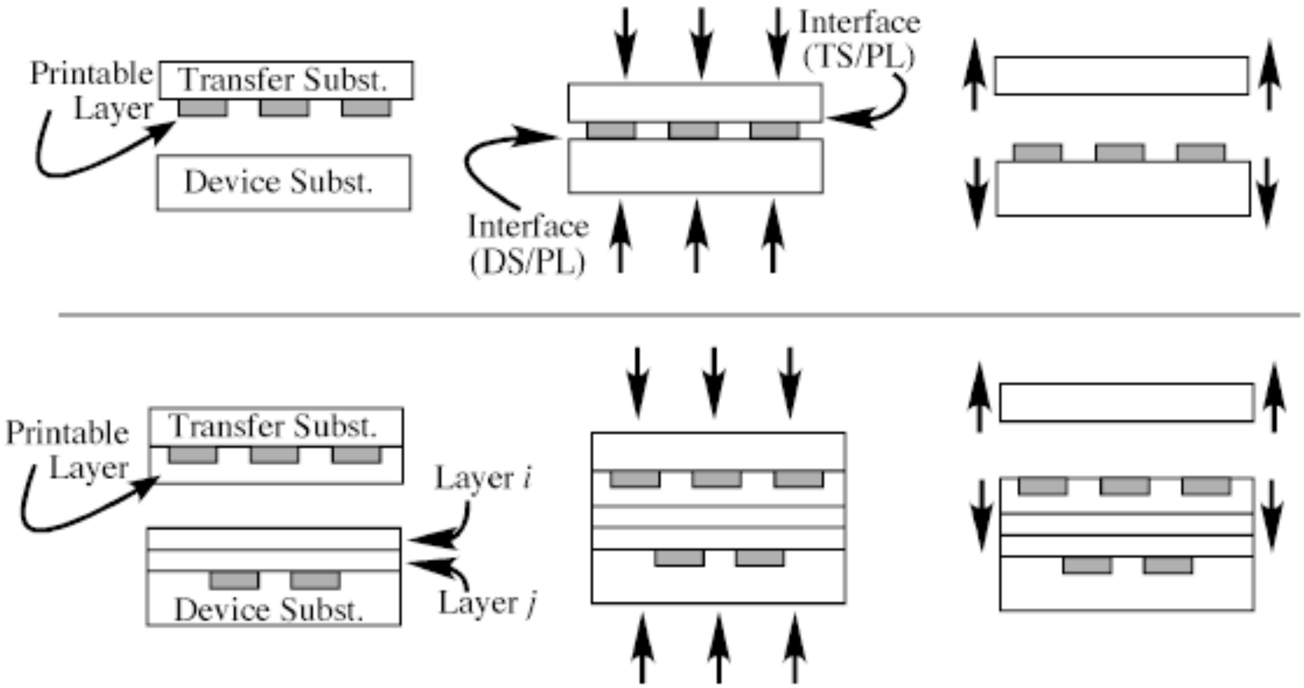
CVD grown Tubes/ PET subst

Spray coated tubes/ PC Subst.



D. R. Hines et. al., Proc. SPIE 6658, 66580Y (2007)

Adhesion Requirements for Transfer Printing



$W_A(DS/PL) > W_A(TS/PL)$

$W_C(DS)$ & $W_C(TS) > W_A(DS/TS)$

$W_A(TS/PL) < W_A(i/j)$ & $W_C(i)$

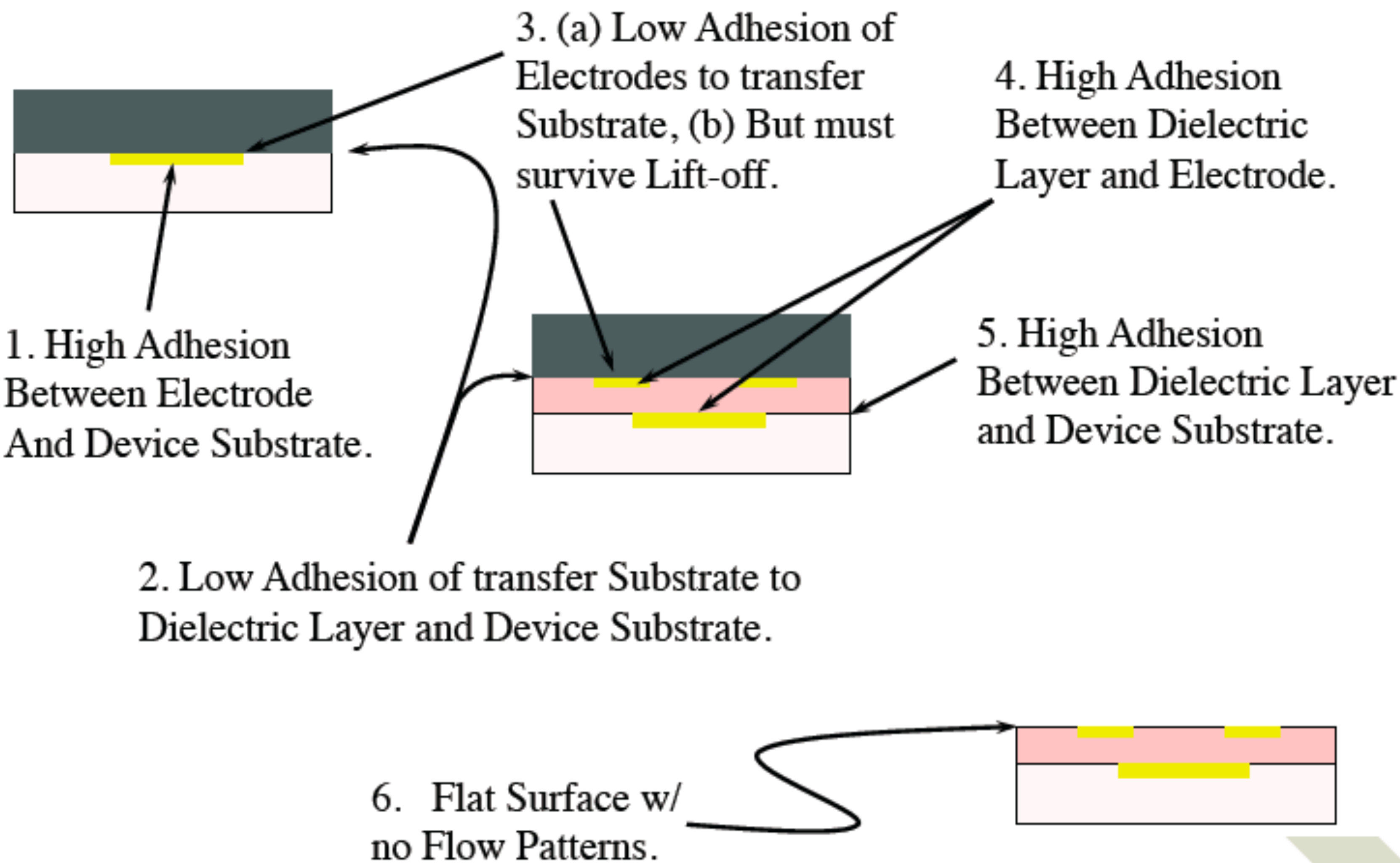
Work of Cohesion & Adhesion:

$$W_C(i) = 2\,\gamma_i$$

$$W_A(i/j) = \gamma_i + \gamma_j - \gamma_{ij}$$

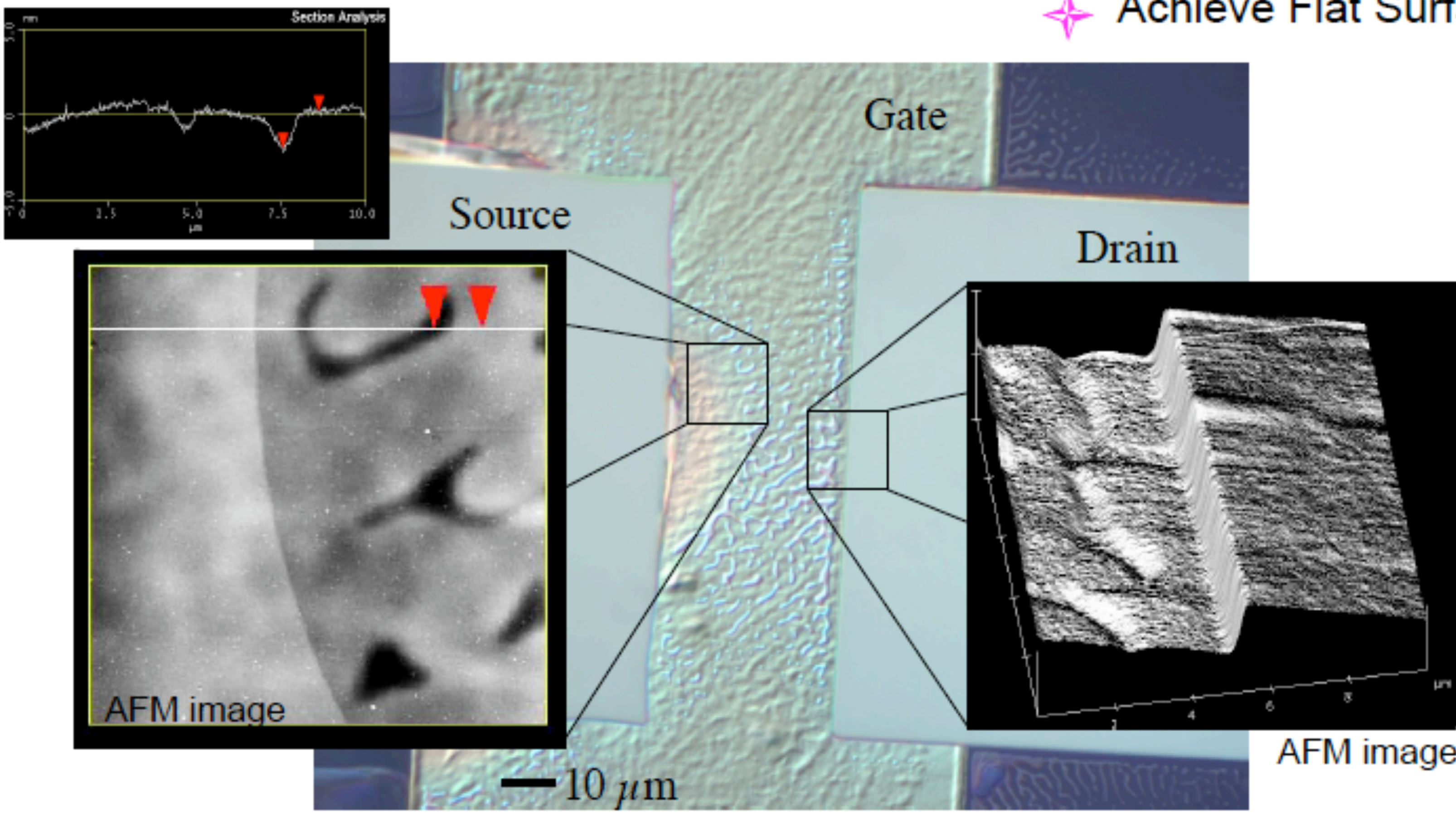
Dupré Equation

Transfer Printing Requirements



Transfer Printing Issues

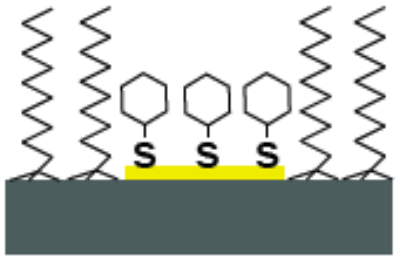
- Eliminate Stress Flow Patterns
- Achieve Flat Surfaces



- High Adhesion between Printable Layer & Device Substrate
- Low Adhesion between Transfer & Device Substrates

Transfer Printing Optimization of Electrode Sub-Assemblies

- 👍 Higher Pressure & Temperature can Alleviate Stress Flow pattern
- 👎 But will Increase Adhesion between Transfer & Device Substrates.



Apply Self-Assembled Monolayers (SAM) to Decrease Adhesion between Transfer & Device Substrates

1. First Protect Au surface w/ BenzeneThiol SAM.
2. Then Apply Release Layer to Si Transfer Substrate.
   (tridecafluoro-1,1,2,2-tetrahydrooctyl)trichlorosilane SAM
3. This allows Higher Temperature & Pressure for Printing Electrodes.
   (500 psi & 170 °C for 3 min.)

Transfer Printing (TP):

- ⇨ Simple & Robust
- ⇨ No Mixed Processing on Device Substrate
- ⇨ No Chemicals used on Device Substrate
- ⇨ Compatible w/ Wide Variety of Materials (both Organic & Inorganic)
- ⇨ Scalable to larger area & roll-to-roll Processing

High Quality Devices On Plastic !

with

Low Contact Resistance

can use

Many Different Materials

TP has been used to Fabricate:

Transistors

Resistors

Capacitors

Vertical Interconnects

Inductors

Transformers

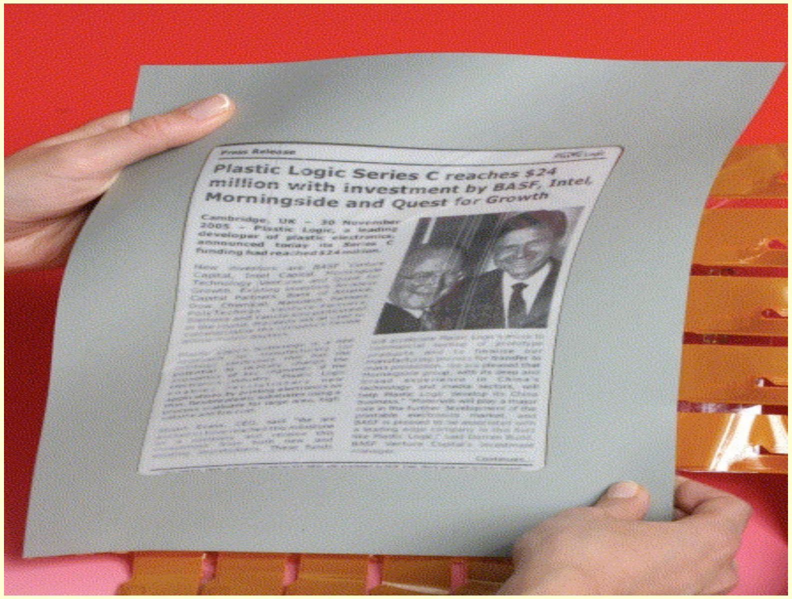
Inverters

Mechanical Resonators

Second Fabrication Technology For Flexible Electronics

- Photolithography: Flexible polymer attached to a silicon carrier substrate (CS).
- Apply traditional processes but at low temperatures.
- Our work is in the area of flexible displays.

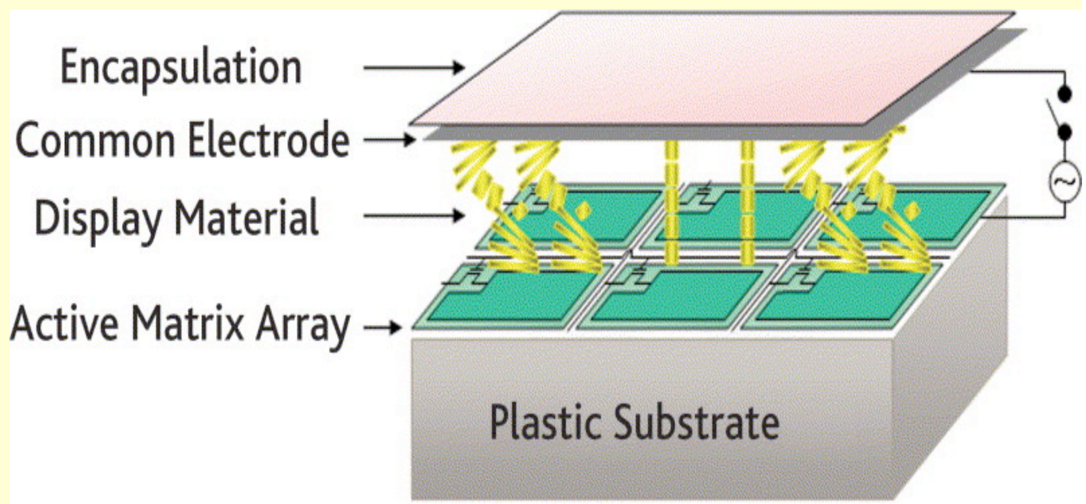
Flexible Displays



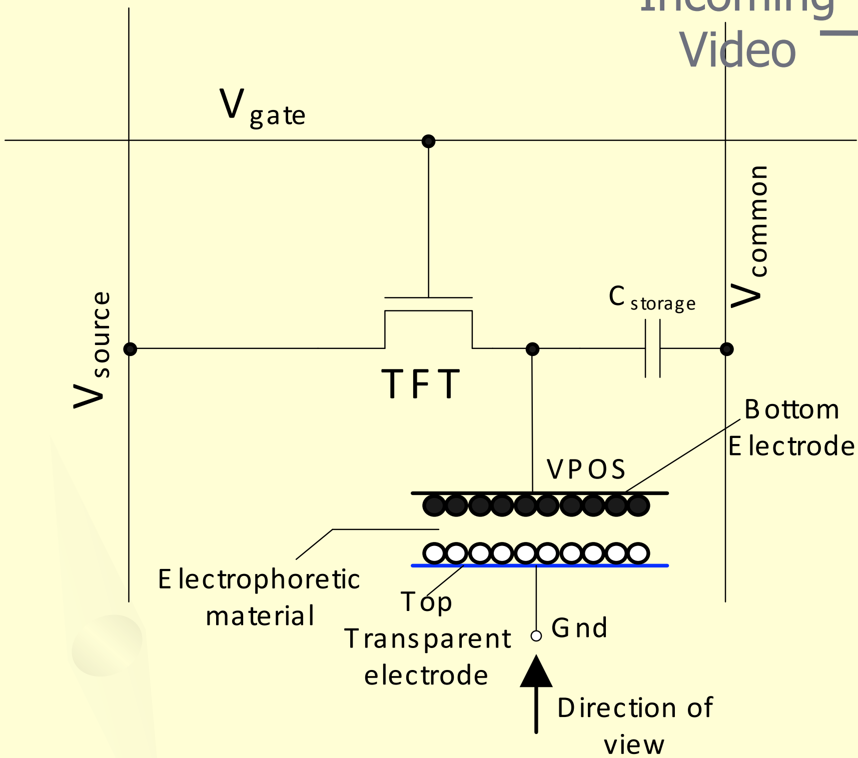
Outline

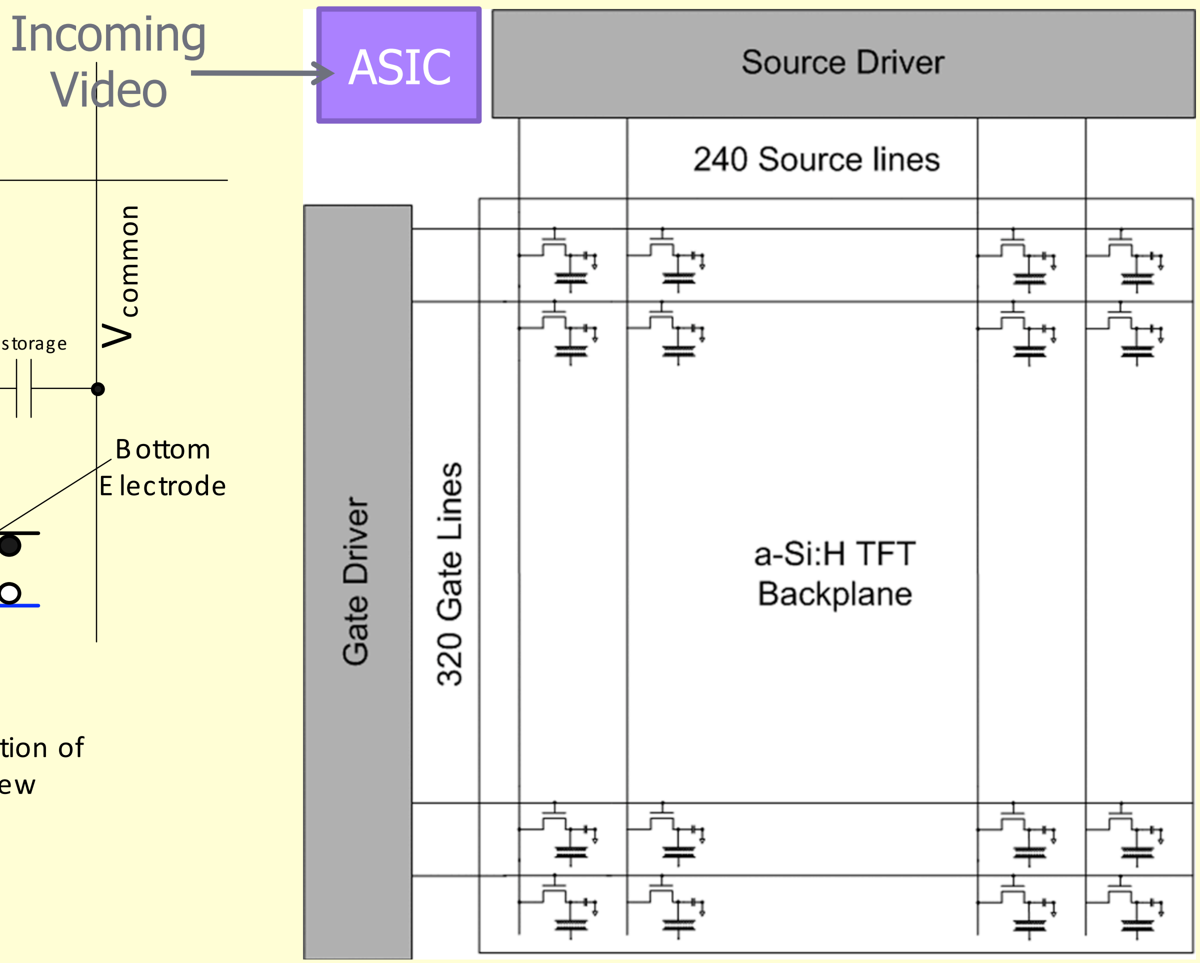
- ►Flexible displays
- ►Previous work: Flexible Substrates and Identification of Problems
- ►Experimental Results: Performance and Reliability
- ►Conclusions

Failure: Lineouts due to cyclical deformation

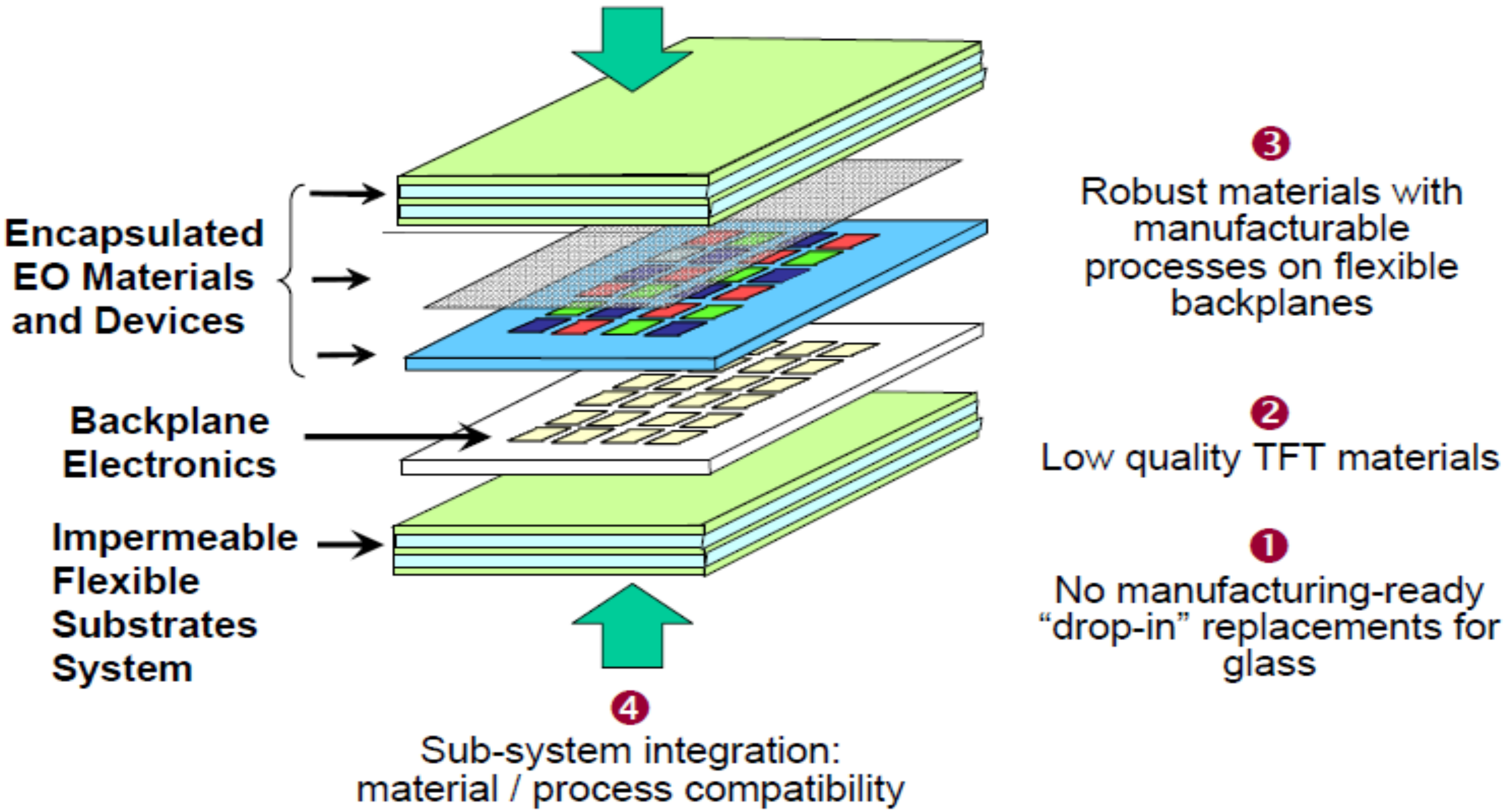


Display Operation
Pixel: TFT and Electro-Optical Material





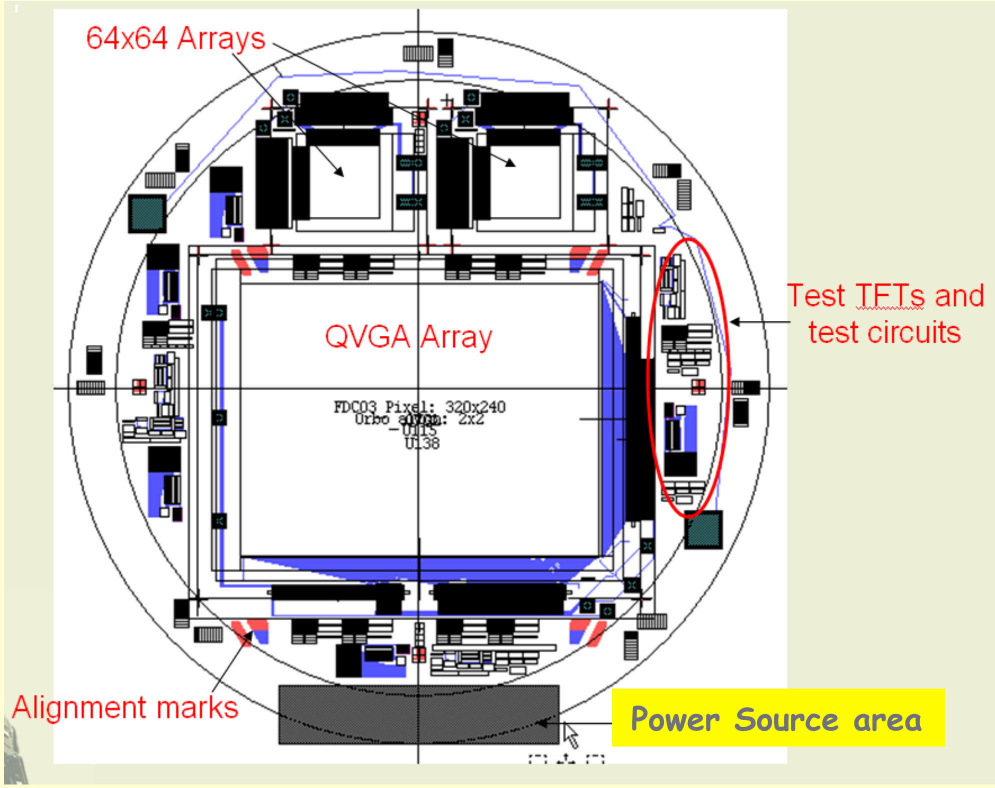
Key technological Challenges



Experimental Approach inorder to resolve the issues

- Process Science and Cell Development with Test Wafer.
- Mechanics of films on flexible substrates
- Specifics of a-Si TFTs
- Metal conductors on a-Si TFTs and power supply for the array.
- Interlayer effects
- Reduction of stress
- Modeling stress effects

Wafer Layout



Low Temp a-Si Process Challenges, Substrate Challenges

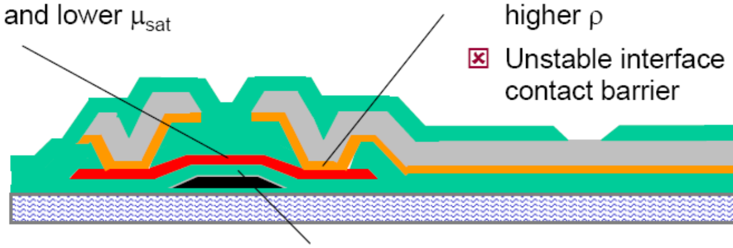
Background and Motivation

- ►Impact of Fabrication process on Performance and Reliability.
- ►3D Integration of a thin film power cell for tft self bias.
- ►Stress build up in hydrogenated amorphous silicon thin film transistors on a flexible substrate
- ►Impact of stresses
  - film delamination
  - cracking / spalling
  - permanent curvature/ warpage of the substrate

Glass-based TFTs
300-350 °C. Process Temperatures → **TFTs on Flex**
175-180 °C. Process Temperatures → **Lower quality active device materials**

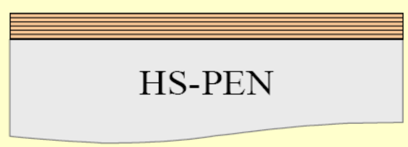
a-Si:H
- ☒ higher SiH_2/SiH ratio → higher V_t and lower μ_{sat}

n^+ a-Si:H contacts
- ☒ unactivated dopants → higher ρ
- ☒ Unstable interface → contact barrier

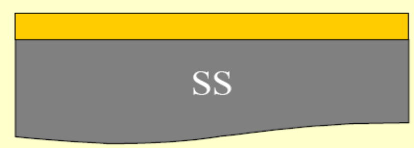


a-SiN_x:H gate dielectric
- ☒ higher charge trap density → greater ΔV_t (stability degradation) and greater hysteresis

HS-PEN
- Process T limits
- Dimensional stability
- Permeable to O_2/H_2O: *barrier layer(s)*

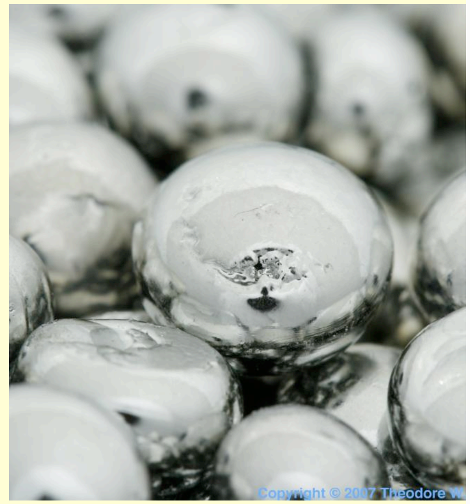


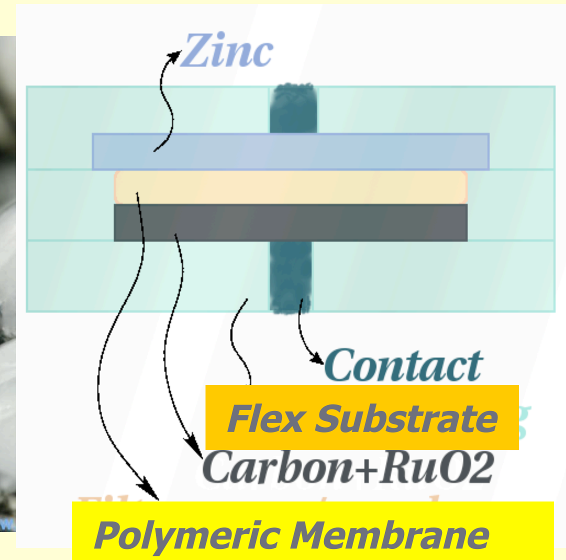
Stainless Steel
- Limited flexibility
- Electrical isolation
- Surface roughness: *planarization layer*

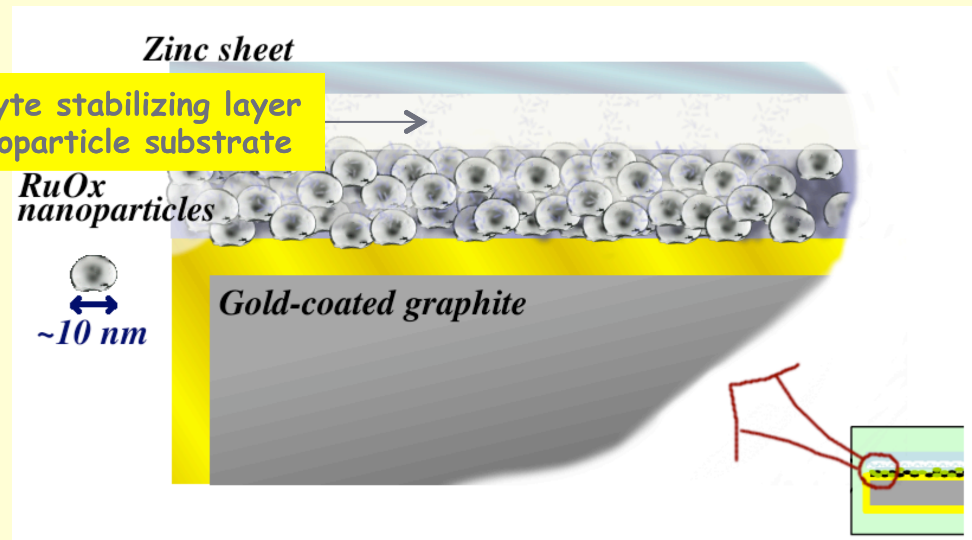


On-Substrate Power Source Technology

- **Cathode**: Mixture of hydrated ruthenium oxide and activated carbon nanoparticles
- **Anode**: Oxidizing metal (zinc, aluminum…)
- **Capped Electrolyte**: Weakly acidic and high viscosity polymer.
- Provisional patents:
  - "Technique for Improving the 'Super-Capacitance' of Ruthenium Oxide Based Capacitors"
  - "A Flexible, High Specific Energy Density, Rechargeable Battery"







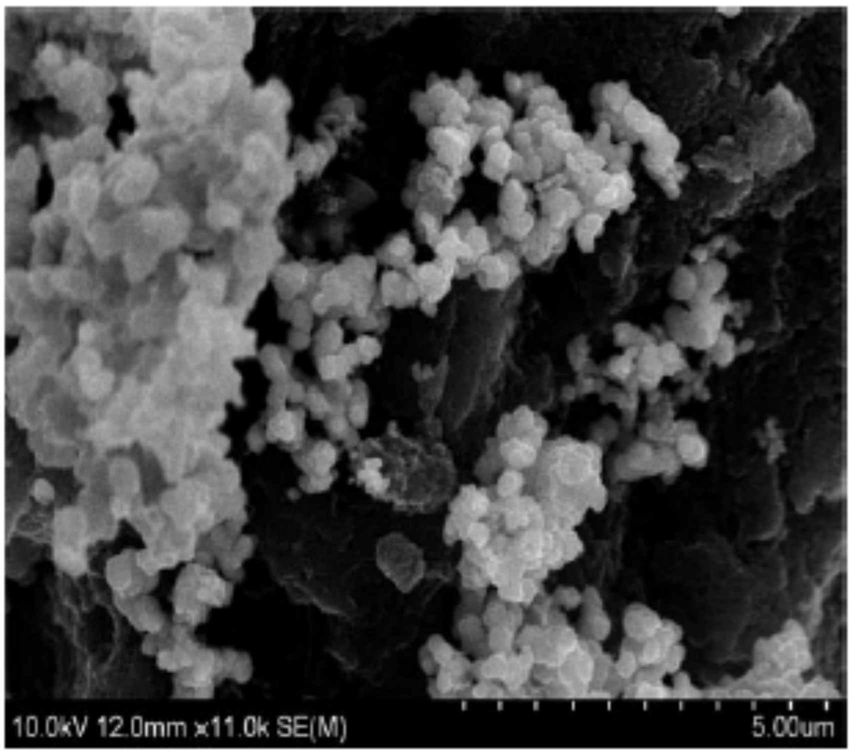
The Basic Redox Reaction

Ruthenium reduced at the cathode Via a surface reaction: $RuO_2 + 2H^+ + 2e^- \rightarrow Ru(OH)_2$

Zinc oxidized at the anode: $Zn \rightarrow Zn^{++} + 2e^-$

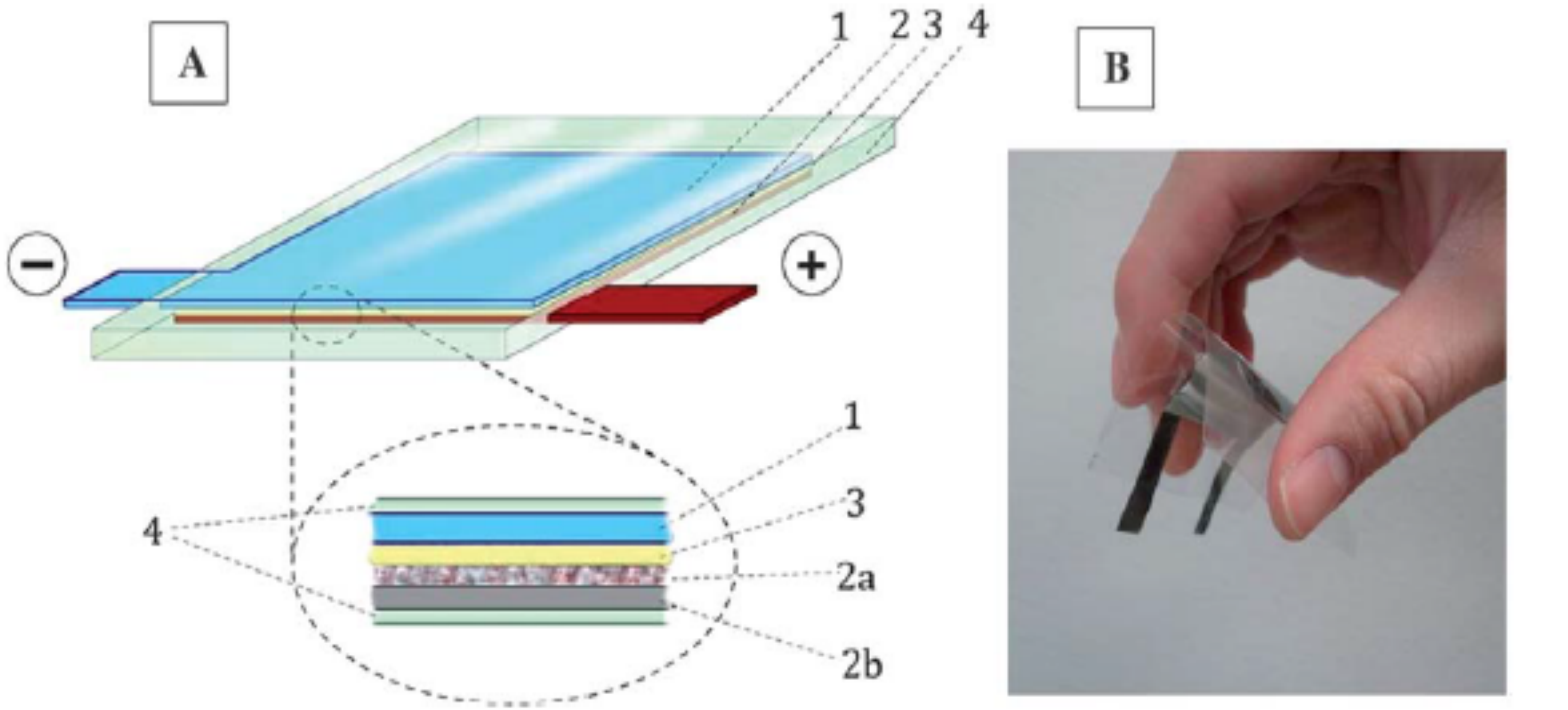
The cathode reaction is purely a surface reaction:
No dissolution of ruthenium occurs

RuO_2-nH_2O Nanoparticles, which decorate activated carbon with a binder (about 500nm diameter)

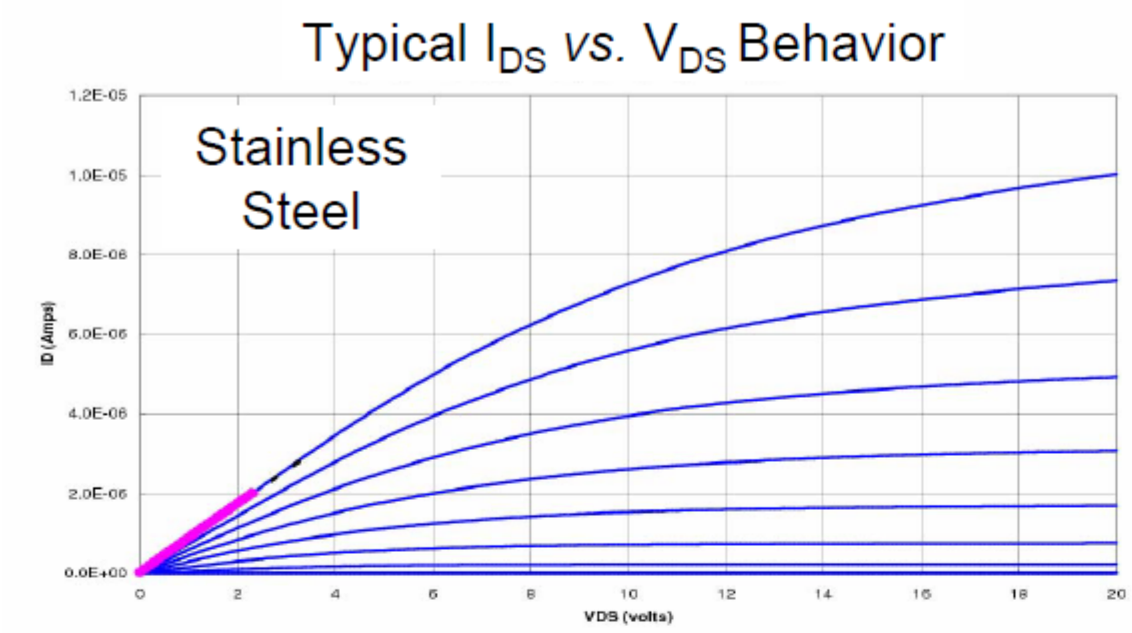


The hydrate, RuO_2-**n**H_2O, is a mixed proton–electron conductor, which can generate an ultrahigh pseudocapacitance.

Cross Section of the single sheet Zn-RuO_2-nH_2O galvanic cell: 1-Zn electrode, 2: RuO_2-nH_2O/activated carbon cathode, 2a-Adhesion layer containing RuOxide nanoparticles, 2b-Graphite film, current collector, 3-separator, 4-packaging substrate



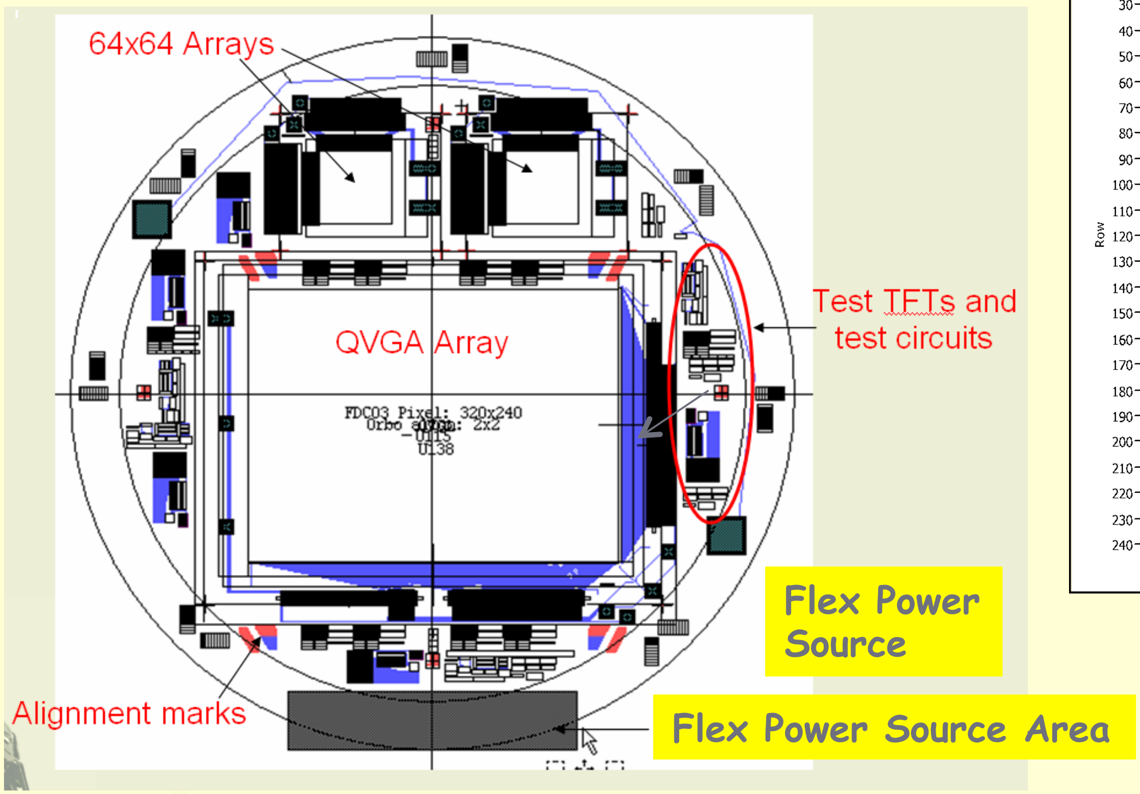
TFT Device Performance

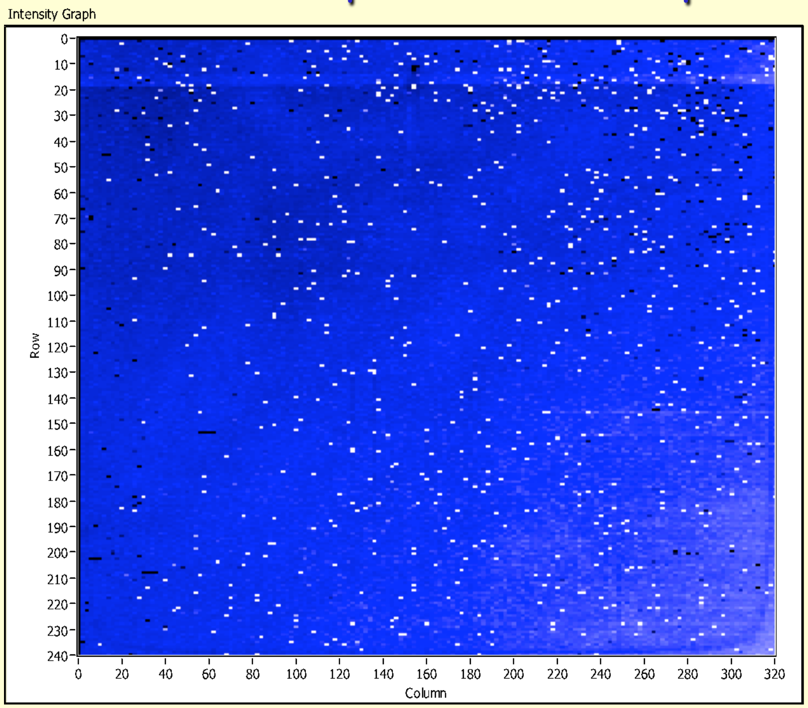


Parameter	Silicon	HS-PEN	Stainless Steel
Saturation Mobility	0.3 $cm^2/V\text{-}s$	0.11 $cm^2/V\text{-}s$	0.20 $cm^2/V\text{-}s$
ON/OFF Ratio	3×10^7	5×10^7	2×10^6
Leakage current	3.3×10^{-13} A	2.8×10^{-13} A	4.9×10^{-12} A
Threshold Voltage	3.00 V	3.68 V	4.09 V

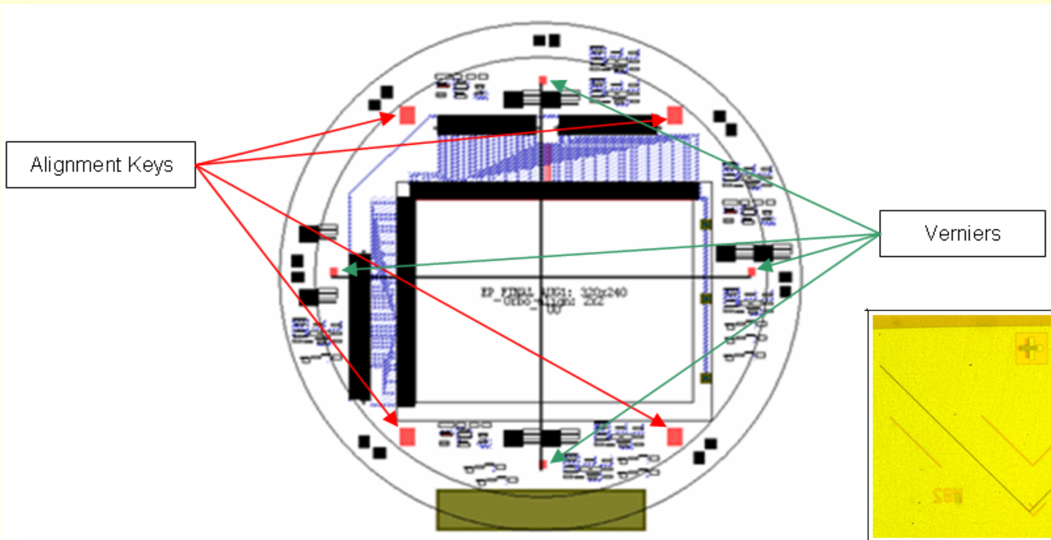
Electrical Measurements: As Processed

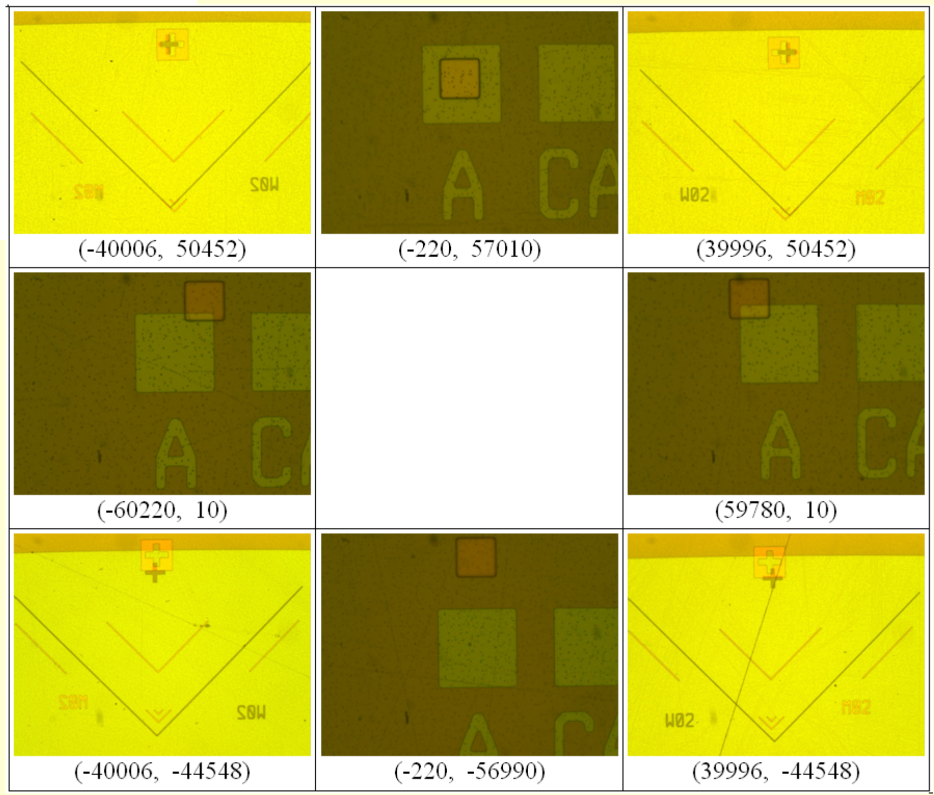
- Drive current across entire array
- White dots represent shorted pixels





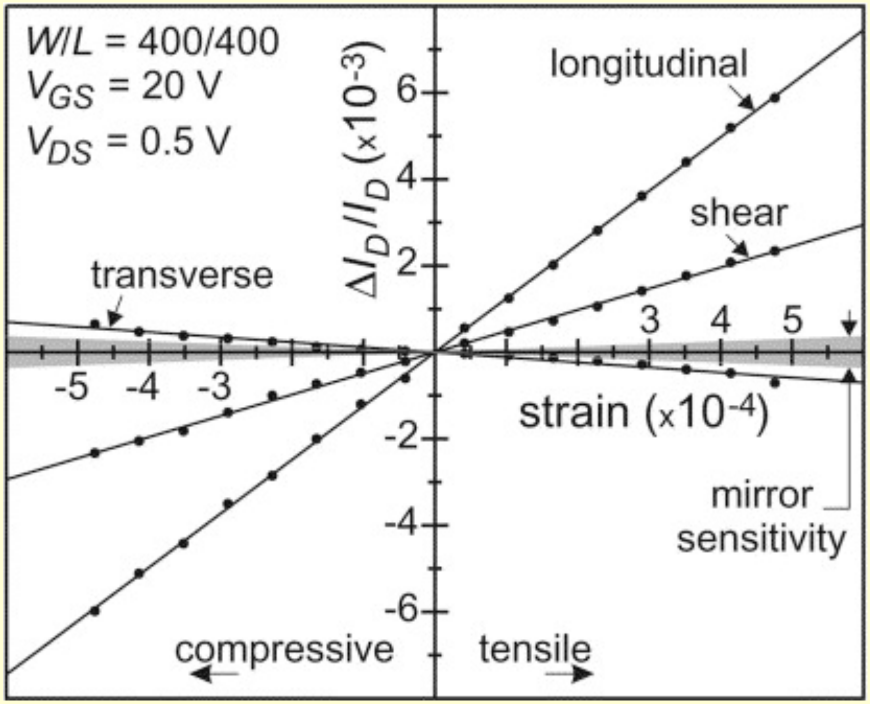
Stress Effects / Distortion: Measured During processing and after thermal degradation, As Processed, 100, 1000 Cycles, 1 hr Period (PEN Substrate)





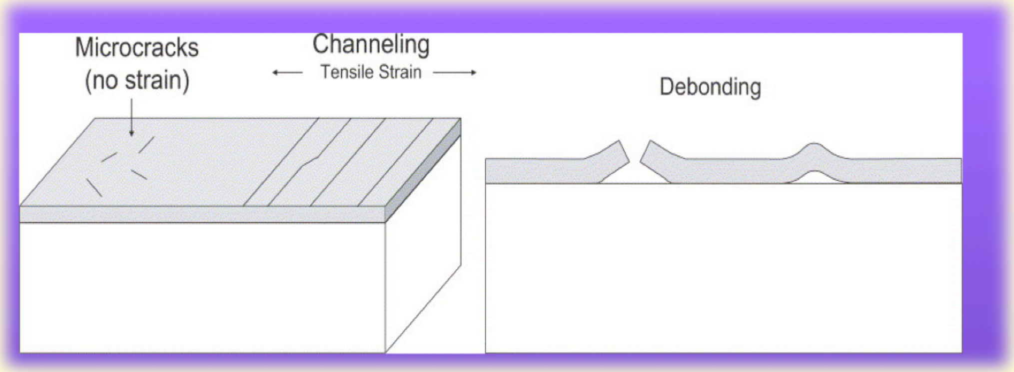
Effect of Strain on Mobility of a-Si TFTs

- Mobility vs strain, ΔT=85C, 100hrs, total, 100 cycles.
- Mobility vs gate orientation
- Performance restored once strain is removed.

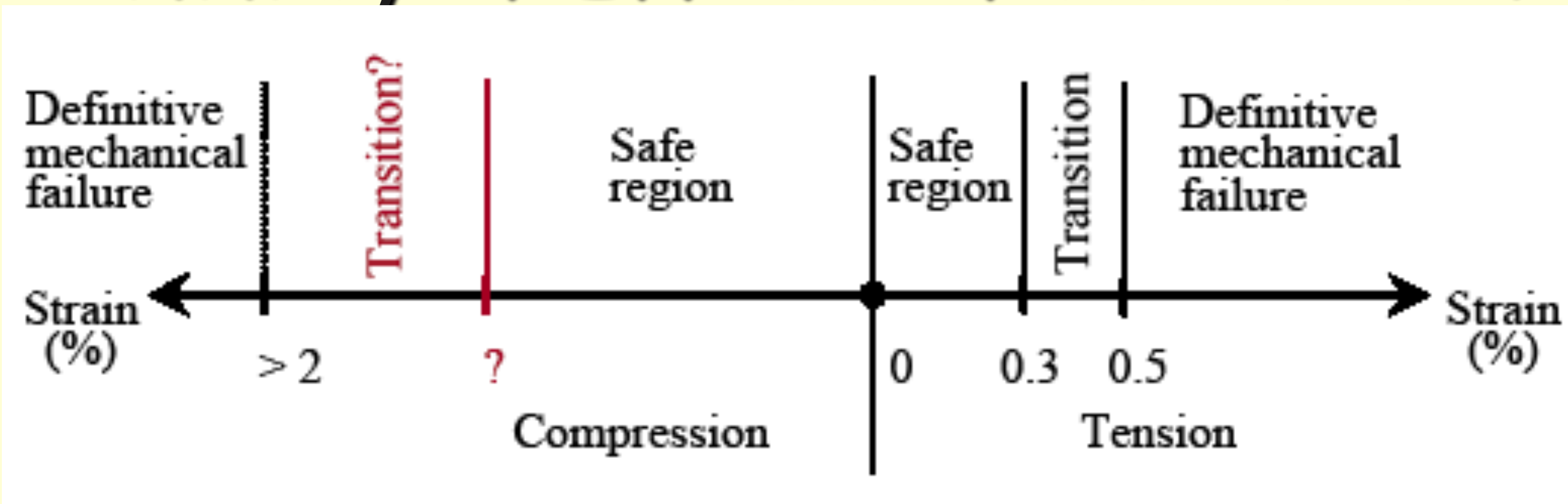


Mechanics of films on flexible substrates:
Temperature Cycling ΔT=85C, 1 hour Periods

►crack networks formed in SiOx coatings on polymer substrates
►PECVD SiOx coatings on PEN substrates
►Failure mode:cracking/ channeling and debonding.



Summary of Effects of strain on TFTs



- Response: elastic deformation -> dielectric fracture
- Electrical function restored once strain is removed
- Compressive strain – mobility reduced
- Tensile strain – mobility increased

Modeling the Mechanical Response

- Internally induced forces
  - Stress from fabrication, Thermal stress, Humidity stress
- Behavior of film/substrate
  - Elastic modulus
  - Thickness of film (d_f), Thickness of substrate (d_s)

Strain: built-in and total

$\varepsilon_M = \varepsilon_0 + \varepsilon_{th} + \varepsilon_{ch}$

ε_M (total mismatch in strain)

ε_0 (built in mismatch in strain)

$\varepsilon_{th} = (\alpha_f + \alpha_s) \times \Delta T$

$(\alpha_f + \alpha_s)$ CTE of film and substrate

ΔT (Tdeposition – Troom)

$\varepsilon_{ch} = -(\beta_f - \beta_s) \times \%RH$

β = coefficient of humidity expansion

Built in Strain

- ε_0 built in during film growth
- Atoms deposited in non-euqilibrium positions
- When deposited on compliant substrate – can produce strong curvature
- Function of RF power during deposition (PECVD)

<u>Determining built in strain & stress</u>

Extracted from radius of curvature

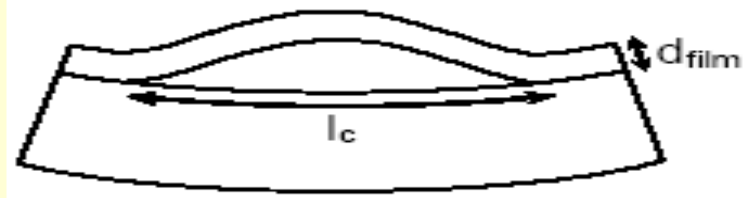
- Measure R
- Determine ε_M from previous equation
- $\varepsilon_M = \varepsilon_0 + \varepsilon_{th} + \varepsilon_{ch}$
- Subtract ε_{th} and ε_{ch}
- Left with ε_0

Then calculate built in film stress

$\sigma_{f0} = [Y_f{*}Ys{*}d_s \;/\; (Y_f{*}d_f + Y_s{*}d_s)] \times \varepsilon_0$

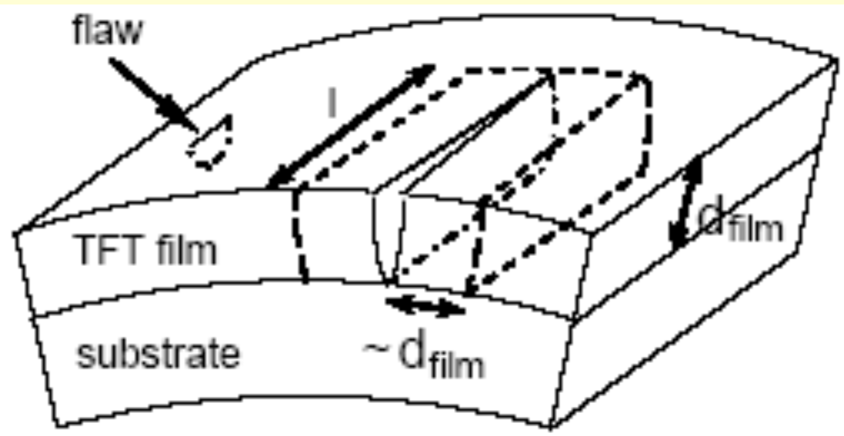
- Pre-existing cracks cause crack propagation
- Condition for crack formation under tension
- Films crack more easily when thickness increased
- Γ specific surface energy
- χ depends on elastic constants of film and substrate

<u>Film/substrate under compression</u>



$$l_c = \frac{\pi d_{film}}{\sqrt{3\left(1-\upsilon_{film}^2\right)}}\sqrt{\frac{Y_{film}}{\sigma_{film}}}$$

Film/substrate under tension



$$2\chi\frac{\left(1-\upsilon_{film}\right)\sigma_{film}^2 d_{film}^2 l}{Y_{film}} > 2\Gamma l d_{film}$$

Effect of substrates

- Film will conform to the substrate
- Biaxial stress arises in plane of film
- Correlation to mismatch strain
  - $\sigma_f = \varepsilon_M Y_f^*$, Y_f^* ε_M is the biaxial elastic modulus of film
- Substrate bend with a radius
  - $R = Y_s^* d^2_s / 6\sigma_f d_f$, Stress is determined by measuring radius R

Compliant substrates

•Substrate also deforms – stress in film reduced
If held rigid during fabrication, stress defined as:

$$\sigma_f = \varepsilon_M Y_f^* / (1 + Y_f^* d_f / Y_s^* d_s)$$

$$\sigma_s = -\sigma_f d_f / d_s$$

•When carrier is removed, has radius of curvature:

$$R = [(Y_s d^2_s - Y^f d^2_f)^2 + 4Y_f Y_s d_f d_s (d_f + d_s)^2] / [6\varepsilon_M Y_f Y_s d_f d_s (d_f + d_s)]$$

Y = plane strain elastic modulus

Summary

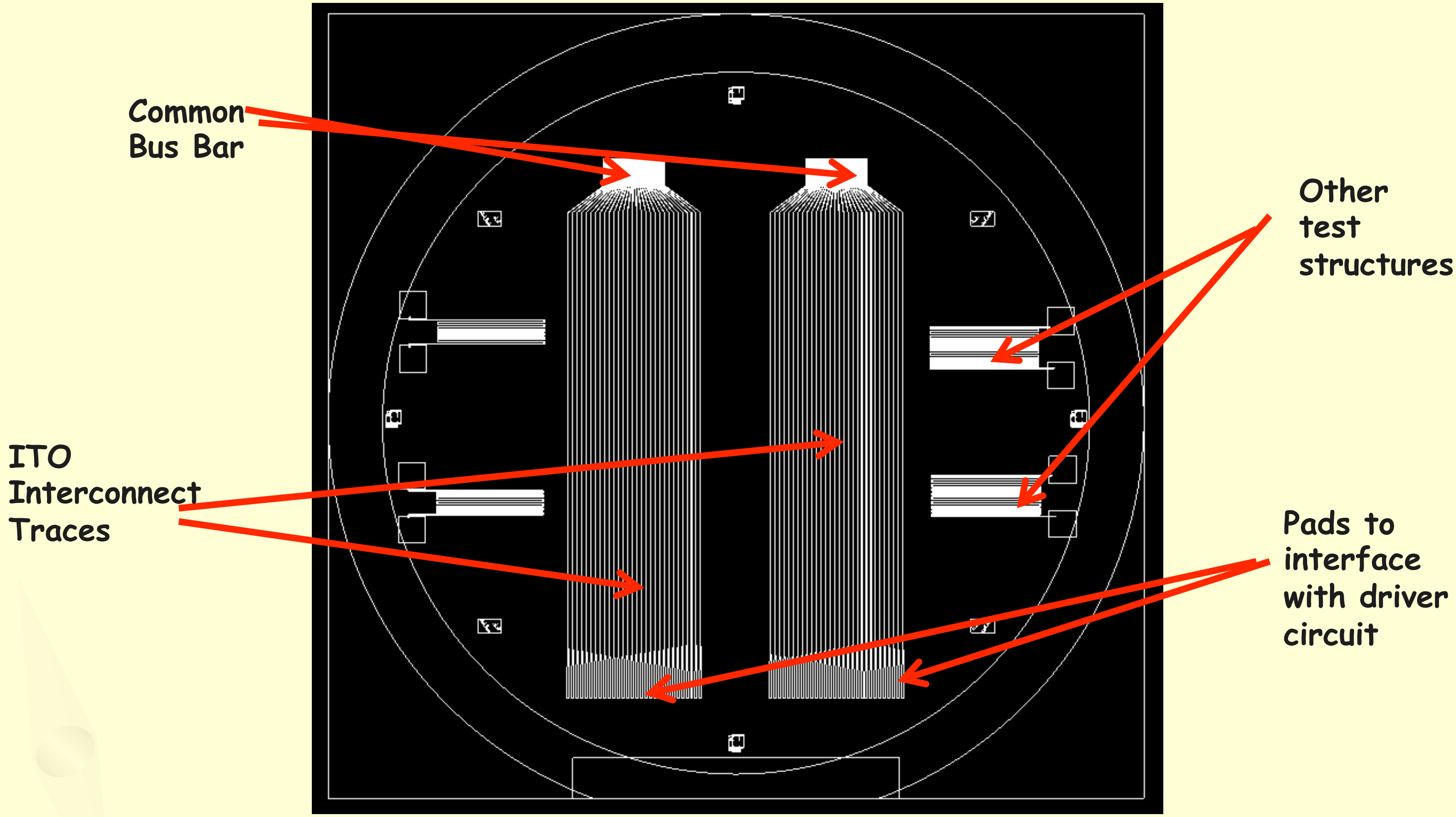
- General approach: Physics of Failure Approach:Mechanical Strain Limits Determined.
- Results of Present Investigation
  - PEN and to be extended to stainless steel
  - Internal stress from fabrication
  - External stress from life testing
    - Power applied
    - Elevated temperature
- Potential problems: Mainly Mechanical

Reliability?

Cyclical Stressing of the substrate results in the main cause of failure.

- Design and integrate a test system to capture time to failure data of thin film interconnects deposited on flexible substrates
- Develop a model to predict cycles to failure based on flexing a substrate to a set radius of curvature.

Wafer Test Structures For Fatigue Investigations

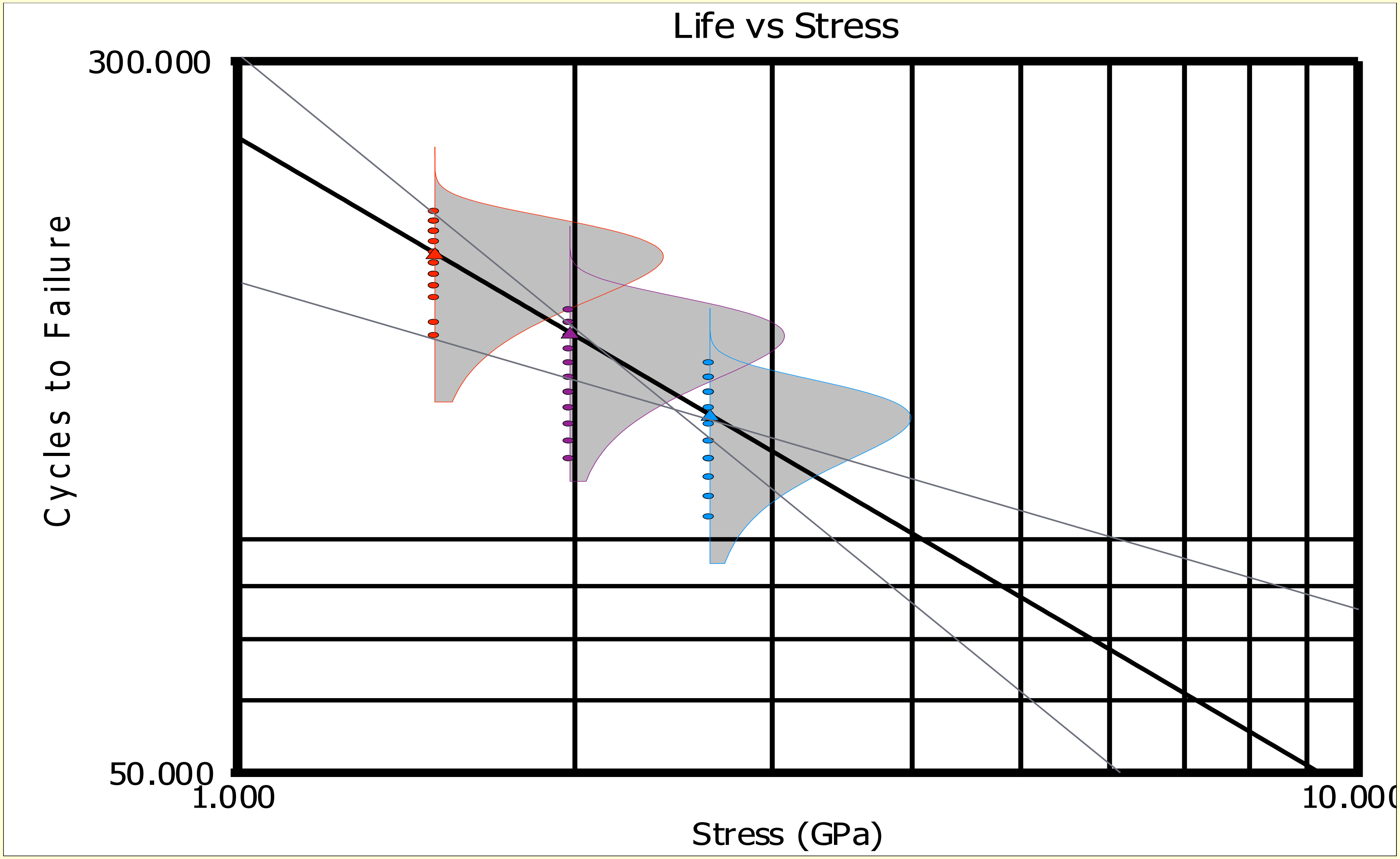


Layer	Thickness (μm)	Process	Process Temp (°C)
ITO	0.05	DC Magnetron Sputtering	98
SiN	0.3	PECVD	180
Planarization	2	Spin coat	230
PEN substrate	125	N/A	N/A

Stress-Number of Cycles to Failure

$$f(t,V) = \beta K V^n (K V^n t)^{\beta-1} e^{-(K V^n t)^\beta}$$

Model parameters estimated from TTF data using Maximum Likelihood Estimation (MLE)



Conclusions

- Cyclical Mechanical stress imposed on gate line interconnects root cause of reliability limitations of flexible displays
- Test system designed to capture TTF of interconnects traces subjected to stress
- Life-stress model has been developed to predict reliability of display bent to a set radius of curvature. Fatigue curves developed.

Acknowledgements: Industrial Funding (L-3 Communications and The Display Consortium)

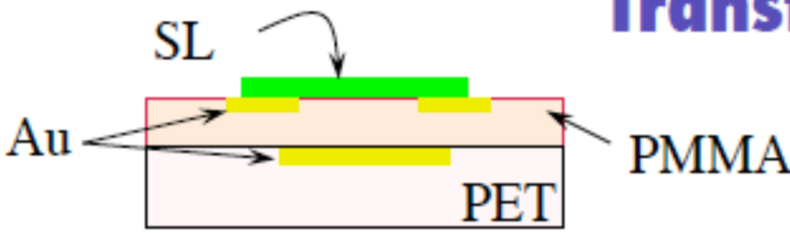
Future Work

- Different materials
  - Carbon nanotubes
  - Organic materials

- Device geometry (interconnect traces)
  - Accordion
  - Serpentine

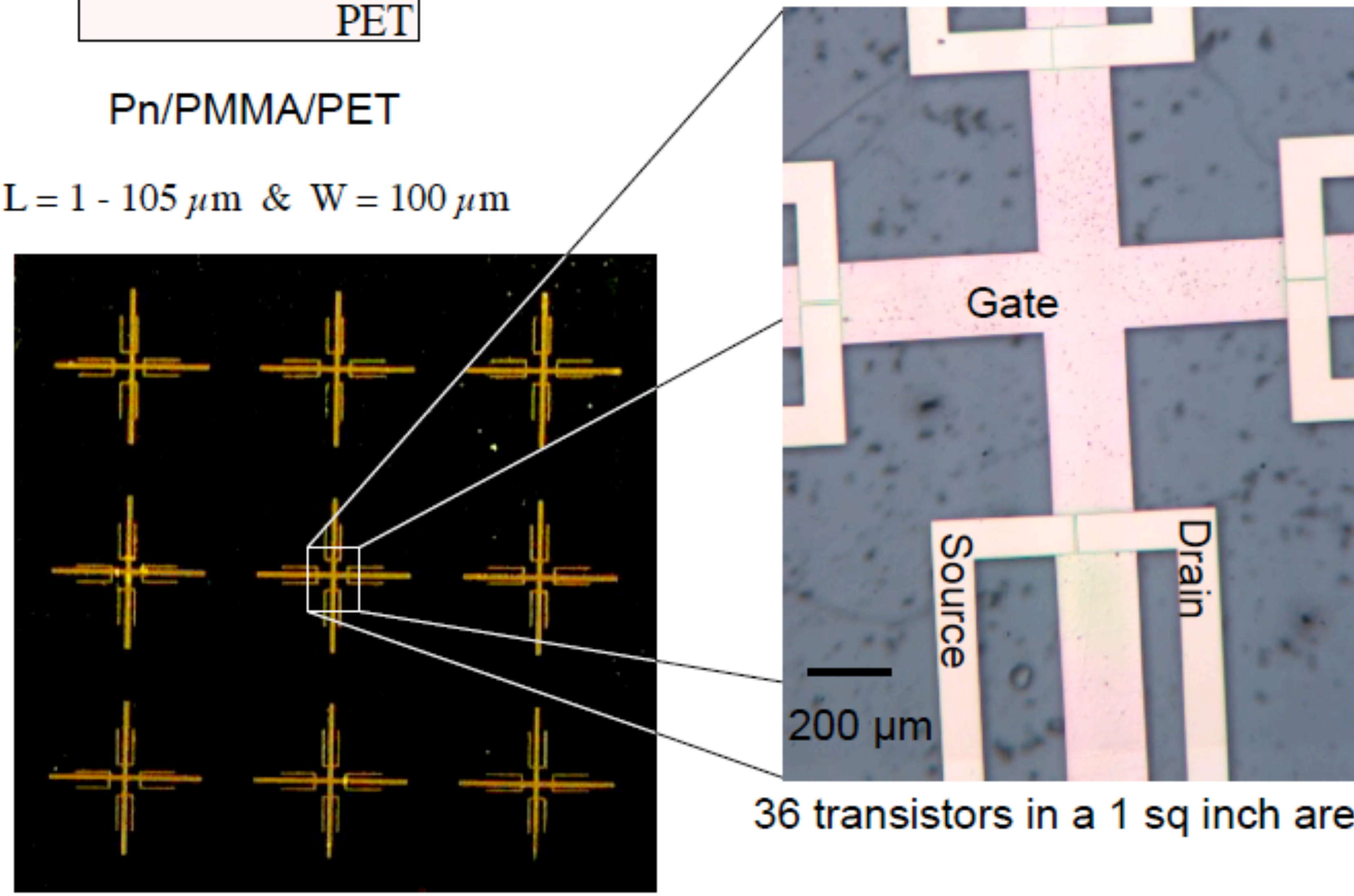
- Fabrication process conditions (lower temp)
- Different processes techniques: Transfer Printing.

Transfer Printed TFTs



Pn/PMMA/PET

$L = 1 - 105\ \mu m$ & $W = 100\ \mu m$



36 transistors in a 1 sq inch area!

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